REMARKS

Applicant thanks the Examiner for acknowledgment of the drawings changes filed on August 4, 2004.

The indication that claim 19 is drawn to the allowable subject matter is also noted with appreciation.

Claims 1 to 8 and 18 to 22 are presently active in the application. By the present amendment claim 1 has been amended in order to better confirm to terminology of the specification and usage in the art and to revise language previously substituted for "sublithographic". The support for the amendment of claim 1 is provided at least on page 1, paragraph 6 of the specification. Claim 6 has been amended to conform to the amendment of December 30, 2003. No new matter is presented by this amendment. The Examiner is respectfully requested to reconsider this application in view of the above amendment and further remarks.

Prior to the rejection discussion the Applicant would like to point out to the Examiner that the reference to Adan et al., which the Examiner mentions in the statement of the rejections of claims 3 and 4-8, but does not identify in the office action or form PTO-892, is not mentioned or evidently relied upon by the Examiner. Therefore, and as suggested in a discussion with Supervisor Examiner Lee and confirmed by the Examiner on January 24, 2005, it is assumed that the inclusion of reference to Adan et al. is in error. Supervisor Lee also confirmed that should the Examiner identify and apply Adan et al. in a future action, such action should not be made final.

Claims 1, 2, 18, and 20-22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Battersby et al. (U.S. Patent 5,528,065) in view of Liao (U.S. Patent 6,180,477). This rejection is respectfully traversed based on the following discussion.

The present invention aims to provide a self-aligned dual gate field effect transistor with a channel region which is sub-lithographic in dimensions without increased source-drain resistance and with reduced gate-junction capacitance and allowing independent control of both gates. The claimed invention presents a

transistor with an appropriate gate thickness in order to avoid gate to junction capacitance and reduce source to drain resistance. Additionally, the claimed conduction channel comprises monocrystalline structure which can guarantee uniform electrical characteristics of the device as a whole.

The patent to Battersby et al. discloses a dual-gate field device such as a MOS tetrode with an active area in which adjacent source regions are separated by and spaced apart from an intervening drain regions. The invention to Battersby et al. aims to reduce a leakage current which is considerably greater in self-aligned technology devices with a plurality of insulated gate sections. The leakage currents of interest in Battersby et al. take place in the ends of the insulated gates wherein the insulated gates extend onto the surrounding insulating region. Additionally, many parallel-connected insulated gate sections, can significantly increase the gate capacitance. Therefore, in order to reduce both the leakage currents and parasitic capacitance, Battersby et al. provides a semiconductor device with insulated gate field, having a semiconductor body wherein one major surface of an active device area is bounded by an insulating region. This approach is quite different from the claimed invention wherein the gate length is anticipated to be shorter than the monocrystalline channel region. The device shown by Battersby has a physical dimension of the monocrystalline region essentially of the entire substrate thickness.

Please note that by this amendment claim 1 has been amended to correct previously added limitation about conduction channel of a first thickness and a dual-gate of 100 nm or less" as it described in the specification page 1, paragraph [0006]. With this change, the reference to Battersby et al. cannot provide the sufficient support for the rejection at least for two reasons.

First of all the monocrystalline channel region shown by Battersby et al. is far thicker than 100 nm, as claimed for the present invention. Applicant also assumes that double-gate structures such as are provided in the present invention can be confusing because of the rotated gate orientation. The standard FET nomenclature now adopted in the claims is as follows: the monocrystalline region

of a transistor would have a length (in the direction of carrier flow and parallel to the gates/dielectrics), width (perpendicular to carrier flow, but parallel to the gates/dielectrics (parallel to the substrate surface in Battersby et al. but vertical or perpendicular to the substrate surface in the in the invention) and thickness (perpendicular to carrier motion and perpendicular to the two gates/dielectrics perpendicular to the substrate surface in Battersby et all. but parallel thereto, transverse to the channel, in the invention).

Applicant respectfully points out that the Examiner appears to be mistakenly using the FET device length and calling it the monocrystalline conduction channel width (thickness). For instance, on page 2 of the Office Action the Examiner refers to the channel width in Fig. 5 as being smaller than the gate highlights the confusion that the FET length and the gate overlaps the channel region horizontally in prior FET structures. In the claimed invention, the corresponding dimension of the monocrystalline channel region extends in the vertical direction. In regard to this structure the Battersby et al. provides no discussion of making this area particularly thin (e.g. vertically in Battersby et al.) to improve control of off-current (leakage).

Furthermore, the usage of the term "width" in the claimed invention has established meaning in FET devices as being parallel to the gate, which is why Battersby et al. recites, " Each drain region 6 is associated with an additional source region 50 provided within the active area 3 spaced apart from the drain region 6 in a direction parallel to the width W of the conduction regions 7 to define an additional conduction region 70..." (Column 5, lines 3-6, emphasis added). Here, Battersy et al. uses the standard definition of device width (e.g. in the plane of the substrate surface) and in this case, the width of the conduction channel is approximately the full long dimension of the drain region 6A in Figure 2. This is very wide in comparison with claimed 100 nm (thickness) claimed by the Applicant in any groundrule set that is physically realizable.

The second reason why Battersby et al. cannot support the rejections is that there are no polysilicon gates on opposing sides of the conducting channel but

merely at the edges thereof and in the same plane. Again, for the Battersby et al. patent to be relevant there would have to be a gate under the channel 7 in Figure 5 so that it could be on opposing sides.

Summarizing the above arguments, Applicant would like to point out that the gate length of the claimed invention is shorter than the monocrystalline channel region and recessed from the source and drain, as claimed. Such proportion is not achievable by the patent to Battersy et al. The physical thickness dimension of the monocrystalline region in the Battersby patent is essentially the entire substrate thickness. The Examiner states in paragraph 6 on page 3 of the office action that the reference to Battersby et al. "discloses that the long dimension (width) of the conduction channel (Col. 9, lines 16-17) exceeds the first width (length) (distance between source and drain by a factor of more than four times". Responding to this argument the Applicant submits that the present invention now refers to the thickness of the conduction channel, not the FET device width or length. The fact that the claimed invention provides the conduction channel thickness to be less than 1/4 the gate length is a significant limitation not shown by the reference to Battersby et al. and from which Battersby et al. teaches away in order to achieve high current, capability of the FET (see column 6, lines 26-29, evidently cited by the Examiner, in which a width possibly 2 500 times the gate length is suggested). In the paragraph 7 of the office action the Examiner states that insulating material between source and drain is shown by Battersby et al. in Figure 5. Responding to this argument the Applicant asserts that there is no polysilicon recess anywhere in Battersby's device or description. The Examiner refers to Figure 5, but insulated gates 11 and 12 are planar everywhere therein.

The Examiner relies on the reference to Liao in rejecting of claim 2, as showing silicide sidewalls. However, as it was discussed above, claim 2 is dependent from claim 1 which is distinguishable over the primary reference to Battersby et al. The patent to Liao does not make up for the deficiencies of the Battersby et al. Therefore the rejection of claims 1, 2 ,18, and 20-22 over

Battersby et al. and Liao should be withdrawn in a view of the present amendment and discussion.

Claim 3 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Battersby et al. in view of Liao and Adan et al. (sic-see above) as applied to Claims 1, 2, 18 and 20 -22, and further in view of Mizuno et al (U.S. Patent 5,844,278). This rejection is respectfully traversed.

The references to Battersby et al. and Liao have been distinguished above. The Examiner relies on patents to Mizuno et al. as disclosing that the polysilicon gate regions are connected with a polysilicon strip at the top. However, as it was pointed out above the primary reference to Battersby et al. cannot support the rejection and therefore the patent to Mizuno et al. cannot make up for the deficiencies of Battersby et al. only by showing connections of the polysilicon gate regions with polysilicon strips.

Claims 4 to 8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Battersby et al. in view of Liao, Mizuno et al., and Adan et al. (sic-see above), as applied to Claims 1-3, 18 and 20-22, and further in view of Liu et al. (U.S. Patent 6,380,078). This rejection is respectfully traversed.

In rejecting of claims 4 and 5, the Examiner relies on the patent to Liu et al. as disclosing a method for forming damascene interconnectors. However, as it was discussed above the primary reference to Battersby et al. does not provide sufficient support for rejection and the reference to Liu et al. cannot make up for the deficiencies of Battersby et al. and therefore the rejection of claims 4 to 8 should be withdrawn.

It is also noted that the Examiner asserts that previously presented remarks are non-persuasive since the claims do not recite any dimensions to be "sublithographic". In this regard, the term "sublithographic" has been the basis for objection and as a result, a definition of that term was substituted for that term in claim 1. Language of that definition has been simplified in the above amendment to even more clearly indicate that the channel thickness is, in fact, sub-lithographic and has been defined as such in claim 1 at a all times during the prosecution of

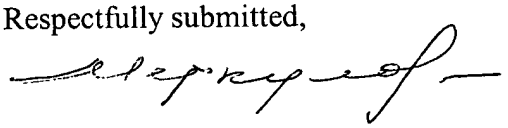
this application.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1 to 8 and 18 to 22 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No.09-0456 (International Business Machine Corporation, Burlington).

Respectfully submitted,



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